Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WOLFDIETRICH G. KASPERKOVITZ and CICERO S. VAUCHER,

Appeal No. 2001-0583
Application No. 09/039,348

ON BRIEF

Before HAIRSTON, KRASS, and SAADAT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 and 4-8, all of the pending claims.

The invention is directed to a receiver tuning system. In particular, a tuning oscillator is synchronized with a stepped-frequency signal having a frequency which can be varied in steps. As depicted in Figure 5 of the application, the tuning signal (in-phase and quadrature mixing signals) is generated in a synchronization circuit LOOP in cooperation with a synthesizer circuit SYNTH, in response to tuning command data

TCD which defines the desired signal to be received. SYNTH generates a stepped-frequency signal Ssf which has a frequency varying in steps, and the LOOP circuit synchronizes a local oscillator LO with the stepped-frequency signal to form a tuning frequency (in-phase and quadrature mixing signals), in which there is an adjustable integer frequency relationship between the stepped-frequency signal Ssf and the tuning frequency. The step size of Ssf is varied in dependence on the adjustable integer frequency relationship such that the tuning frequency has substantially uniform steps.

Representative independent claim 1 is reproduced as follows:

> 1. A receiver comprising a tuning system for tuning the receiver, the tuning system comprising:
>
> a frequency-synthesis circuit for generating a stepped- frequency signal having a frequency varying in steps with a step size; and
>
> a synchronization circuit for synchronizing a tuning oscillator to the stepped-frequency signal to form a tuning frequency, said synchronization circuit comprising means for providing an adjustable integer frequency relationship between the stepped-frequency signal and the tuning frequency,
>
> characterized in that the frequency-synthesis circuit comprises means for varying the step size of the stepped-frequency signal in dependence on the adjustable integer frequency relationship such that the synchronization circuit forms the tuning frequency having substantially uniform tuning steps.

The examiner relies on the following reference:

Gilmore	4,965,533	Oct. 23, 1990

Claims 1 and 4-8 stand rejected under 35 U.S.C. 102 (b) as anticipated by Gilmore.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

At the outset, we note that, in accordance with appellants' grouping of the claims at page 3 of the brief, all claims will stand or fall together.

It is the examiner's position that Gilmore teaches a frequency synthesizer 102 for generating a stepped-frequency signal, which is the input to 116 of PLL 114. The examiner contends that this stepped-frequency signal varies in steps with a step size, explaining that the step size of the signal input to phase detector 116 of PLL 114 varies with the divisor value of the loop divider 122. Actually, the stepped-frequency signal input to phase detector 116 from DDS 102 is not varied at the input but the reference signal from DDS 102 is modified in the phase detector 116 in accordance with the signal from loop divider 122. The examiner also contends that PLL 114 is the claimed synchronization circuit and that it comprises a means 122 for providing an adjustable integer frequency relationship between the step-frequency signal and the

tuning frequency. The tuning frequency is the output of PLL 114 and the examiner contends that this tuning frequency has substantially uniform steps of 10MHz, citing

column 6, lines 41-48, of Gilmore.

For their part, appellants contend that it is the output tuning frequency of the Gilmore PLL 114 which has a variable step size over the output frequency range. In comparison, the instant claimed subject matter requires the frequency synthesizer circuit to have the "means for varying the step size of the stepped-frequency signal in dependence on the adjustable integer frequency relationship such that the synchronization circuit forms the tuning frequency having substantially uniform tuning steps" [brief-page 4].

Appellants contend that this is "the opposite" of what is taught by Gilmore because instant claim 1 relates to a stepped-frequency signal from the frequency-synthesis circuit which is then applied to the synchronization circuit which, in turn, generates a tuning frequency which has uniform tuning steps, whereas "Gilmore does not show or suggest that while the stepped frequency signal, which is used to generate the tuning frequency, has a variable step size, the resultant tuning frequency signal has a uniform step size" [brief-page 5].

We agree with the examiner.

Perhaps the examiner's position, as we view it, can best be explained if we view Gilmore's Figure 2 with a box around DDS 102, filter 110, optional divider 112 and phase detector 116. Then, the rest of the elements, filter 118, VCO 120 and divider

122, constituting PLL 114, would have a box drawn around them. The circuit function doesn't change and the relationship between the elements does not change, merely the nomenclature of the circuit which contains the phase detector would change.

In this case, it can clearly be seen that Gilmore discloses a frequency-synthesis circuit for generating a stepped-frequency signal having a frequency varying in steps with a step size (the top input to phase detector 116). It also discloses a synchronization circuit (elements 118, 120, 122) for synchronizing a tuning oscillator VCO 120 to the stepped-frequency signal (upper input of phase detector 116), wherein the synchronization circuit comprises means for providing an adjustable integer frequency relationship between the stepped-frequency signal and the tuning frequency (loop divider 122 takes the tuning frequency, i.e., output of VCO 120, and varies the stepped-frequency with this tuning frequency in phase detector 116 such that there is the integer frequency relationship claimed) characterized in that the frequency-synthesis circuit comprises means for varying the step size of the stepped-frequency signal (this is phase detector 116) in dependence on the adjustable integer frequency relationship (adjustable by divider 122) such that the synchronization circuit forms the

tuning frequency having substantially uniform tuning steps (as indicated at column 6, lines 41-59, of Gilmore, the tuning frequency has uniform tuning steps, e.g., 200, 210 . . . 390, 400 MHz, in dependence on the reference signal, e.g., 10MHz input from DDS 102).

The examiner's decision rejecting claims 1 and 4-8 under 35 U.S.C. 102 (b) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

KENNETH W. HAIRSTON Administrative Patent Judge	)
ERROL A. KRASS Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
MAHSHID D. SAADAT Administrative Patent Judge	)

eak/vsh

U.S. PHILIPS CORPORATION
CORPORATE PATENT COUNSEL
580 WHITE PLAINS ROAD
TARRYTOWN, NY 10591